APPENDIX B

CLEAN VERSION OF SPECIFICATION

Noise Canceling Circuit

1. Field of the Invention

The present invention mainly relates to ripple noise cancellation in a stabilized DC power supply, and particularly provides a power circuit that achieves the high ripple noise cancellation rate with low operating current.

2. Discussion of the Background Art

Not only electronic equipments, but also all the other electronic devices contain a plurality of stabilized DC power supply voltages. The power circuits are disposed in digital circuits, high-frequency circuits and analog circuits, said power circuits having the characteristics suitable for use in these circuits. In a cellular phone, among others, the highest ripple cancellation rate is required because a poor ripple cancellation rate in a power supply of a transmitting section degrades the clarity of the voice conversation. Even in a digitally coded wireless communication means, a carrier signal is modulated and demodulated in an analog manner during the modulation and the demodulation, and therefore the power source ripple noises adversely influence the error rate. As to the cancellation of these ripple noises, for example, the cancellation rate of -80dB can be achieved by causing a sufficient amount of the operating current of 100μA to flow. Though some inventions are proposed as described later, there is no proposal that drastically

reduces the low operating current and realizes the high ripple cancellation rate.

At present, it is assumed that a few billion of such equipments are operated all over the world. In case one power circuit is operated with 200μA, it means that the current of 1,000,000 ampere flows in five billion power circuits. In case one power circuit is operated with 3V, it means that the electric power of 3,000KW is consumed. The prior arts and the circuit theory based on the prior arts will be examined below by referring to the diagrams.

(1) Example of a Conventional Circuit

Figs. 1 and 2 are a block diagram and a circuit diagram of a CMOS-type stabilized power circuit that has been conventionally used. In Fig. 1, the numerals 1 and 2 indicate voltage supply terminals. The numeral 50 indicates a reference voltage generation circuit that generates a reference voltage Vref. The numeral 60 indicates a circuit that generates a bias current for determining an operating current. The numeral 100 indicates an error amplifier circuit that amplifies an error voltage for the reference voltage Vref. The error amplifier circuit 100 is a two-stage amplifier; a differential circuit 10 is the first stage and a phase inversion amplifier 20 is the second stage. The numeral 40 indicates a circuit that detects a fluctuation of the output voltage and divides the voltage. The concrete example of the conventional stabilized

power circuit is shown in the circuit diagram of Fig. 2. The reference voltage generation circuit 50 is connected to an input terminal N1 of the error amplifier, and the output divider circuit 40 is connected to an input terminal N2 of the error amplifier.

Fig. 3 is a graph that shows the DC characteristics in the conventional circuit shown in Fig. 2, showing the dependence on a power supply voltage Vdd by the output voltage Vout and the reference voltage Vref. The horizontal axis indicates the power supply voltage Vdd. The numeral 31 indicate an operating current. The numeral 32 indicates a gate voltage of an output transistor. The numeral 33 indicates the output voltage Vout and the numeral 34 indicates the reference voltage Vref.

Fig. 4 is a 10,000-times-expanded Fig. 3. The numeral 41 indicates the output voltage Vout and the numeral 42 indicates the reference voltage Vref. As shown by the numeral 42, generally, the reference voltage source Vref has a positive source voltage coefficient and has the properties, that as the source voltage rises, the output is increased. These properties are inconvenient for the ripple cancellation rate, whereby particularly the ripple cancellation rate in the low band is to be greatly influenced by the source voltage dependency coefficient of the reference voltage. Though it is not impossible to set the source voltage coefficient to zero, a trimming and a special voltage coefficient element need to be used. Therefore, this

requires very great costs in a widely used semiconductor manufacturing method.

(2) Theoretical Formula of the Conventional Circuit

Next, the theory of the output voltage will be examined. The output voltage Vout is represented by the following formula:

$$Vout = Vref*(Av/1 + K*Av) + So \quad (1)$$

In this formula, Vref indicates the reference voltage, Av represents a voltage gain of the error amplifier, K represents the division ratio of the divider circuit, and So represents a system offset voltage of the error amplifier.

The reference voltage Vref is influenced by the source voltage Vdd. Therefore, the change rate thereof is represented by the source voltage coefficient of Vref, $\Delta Vref = (\delta Vref/\delta v)/K$.

K is the division ratio of an output voltage-division resistance, and $K < 1$. The high PSRR cannot be realized, unless the ripple noise $\Delta Vref$ derived from Vref is rejected by a filter (PSRR means Power Supply Rejection Ratio, the ratio representing how much the output changes when the source voltage Vdd changes by 1V; for example, if the output changes by 1mV, PSRR is 1mV/1V, i.e. -60dB). The ripple noise of Vref contains

a very low frequency and a high frequency component, and therefore a large time constant is required for a filter, whereby a filter rejecting all the frequency bands cannot be integrated on the same semiconductor chip.

In Fig. 4, Vref increases by about 10μV (-100dB), when Vdd is from 4v to 5v (0dB). Vout increases by 90μV (-82dB).

K indicates the division ratio of the output divider circuit and is represented by the following formula:

$$K = R1/R1 + R2$$

Here, R1 and R2 indicate resistors in the output divider circuit. If these resistors are made of polysilicon, the influence of Vdd can be neglected. Therefore, the rate of change of the source voltage Vdd is not taken into consideration. The value of K is a division value that determines the output voltage. Vref is generally from 0.2 to 0.8, and an extremely small or large value cannot be determined. Thus, this value contributes to the ripple reduction in a limited manner only.

So in the formula (1) represents the system offset voltage, which is unavoidably generated due to the circuit configuration. The system offset voltage is introduced by assuming its existence from an experimental value, on the basis of a way of thinking that

has never been conventionally employed. It is empirically known that So is influenced by Vdd, and the formula (1) represents that So has a positive coefficient in most cases and, if a negative coefficient is feasible, So plays an important role.

Here, the source voltage coefficient is represented by

$So = \delta So / \delta v.$

Av indicates an amplification factor of the entire circuit, has an open-loop gain and has a dependency on the source voltage Vdd as a matter of course. Therefore, the rate of change is represented by the following differential formula:

$$\Delta Av = (\delta Av / \delta v) / (1 + KAv)^2$$

Incidentally, in case Av = 10,000 times (80dB), K = 0.5, and the source voltage increases by 1V, 10,000 times is changed into 12,000 times, so that δAv = 2,000 times and δV = 1v. Thus,

$$\Delta Av = 80 \times 10^{-6}$$